What is claimed is:

1. A lateral semiconductor device comprising:

a semiconductor chip;

two main electrodes on one major surface of the semiconductor chip; and

an alternating conductivity type layer between the main electrodes;

wherein the alternating conductivity type layer comprises first semiconductor regions of a first conductivity type and second semiconductor regions of a second conductivity type;

wherein the first semiconductor regions and the second semiconductor regions are alternately arranged; and

wherein the alternating conductivity type layer comprises a closed loop surrounding one of the main electrodes.

2. The lateral semiconductor device according to Claim 1, wherein the alternating conductivity type layer comprises first sections, wherein the first semiconductor regions and the second semiconductor regions are arranged alternately at a first pitch, and second sections, wherein the first semiconductor regions and the second semiconductor regions are arranged alternately at a second pitch different from the first pitch.

3. The lateral semiconductor device according to Claim 1, wherein the alternating conductivity type layer comprises at least one straight section and at least one curved section.

4. The lateral semiconductor device according to Claim 3, wherein the alternating conductivity type layer comprises at least two straight sections and at least two curved sections.

5. The lateral semiconductor device according to Claim 4, wherein the alternating conductivity type layer comprises at least four straight sections and at least four curved sections.

6. The lateral semiconductor device according to Claim 3, wherein the first semiconductor regions and the second semiconductor regions are arranged alternately at the first pitch in the straight sections, and the first semiconductor regions and the second semiconductor regions are arranged alternately at the second pitch in the curved sections.

7. The lateral semiconductor device according to Claim 6, wherein the first pitch is equal to or longer than the second pitch.

8. The lateral semiconductor device according to Claim 6, wherein the curved sections are doped substantially more lightly than the straight sections.

9. The lateral semiconductor device according to Claim 8, wherein the curved sections are substantially intrinsic.

10. The lateral semiconductor device according to Claim 8, wherein the first pitch is shorter than the second pitch.

11. The lateral semiconductor device according to Claim 8, wherein the curved sections are doped with an n-type impurity and a p-type impurity.

12. The lateral semiconductor device according to Claim 9, wherein the curved sections are doped with an n-type impurity and a p-type impurity.

13. The lateral semiconductor device according to Claim 3, wherein the width of at least a portion of the curved section is larger than the width of the straight section.

14. The lateral semiconductor device according to Claim 1, further comprising one or more closed loops, each including an alternating conductivity type layer.

15. The lateral semiconductor device according to Claim 1, wherein the width of the first semiconductor region or the second semiconductor region is from 1/4 to 4 times as large as the depth of the first semiconductor region or the second semiconductor region respectively.

16. The lateral semiconductor device according to Claim 1, wherein the width of the alternating conductivity type layer is from 12.5 to 100 times as large as the width of the first semiconductor region or the second semiconductor region.

17. The lateral semiconductor device according to Claim 16, wherein the width of the alternating conductivity type layer is from 12.5 to 100 times as large as the depth of the first semiconductor regions or the second semiconductor regions.

18. A lateral semiconductor device comprising:

a semiconductor chip having two major surfaces;

two main electrodes on one of the major surfaces of the semiconductor chip;

one or more alternating conductivity type layers between the main electrodes, each of the alternating conductivity type layers comprising first semiconductor regions of a first conductivity type and second semiconductor regions of a second conductivity type, the first semiconductor regions and the second semiconductor regions being arranged alternately, the first semiconductor regions provide a current path in the ON-state of the semiconductor device and are depleted in the OFF-state of the semiconductor device, and the second semiconductor regions are depleted in the OFF-state of the semiconductor device; and

lightly doped regions, the impurity concentrations thereof are substantially low;

wherein the one or more alternating conductivity type layers and the lightly doped regions being connected to each other to form a closed loop surrounding one of the main electrodes.

19. The lateral semiconductor device according to Claim 18, wherein the closed loop comprises at least one straight section and at least one curved section.

20. The lateral semiconductor device according to Claim 19, wherein the closed loop comprises at least two straight sections and at least two curved sections.

21. The lateral semiconductor device according to Claim 20, wherein the closed loop comprises four or more straight sections and four or more curved sections.

22. The lateral semiconductor device according to Claim 19, wherein the straight section comprises the alternating conductivity type layer and the curved section comprises the lightly doped region.

23. The lateral semiconductor device according to Claim 18, wherein the surface portion of the lightly doped region is substantially intrinsic.

24. The lateral semiconductor device according to Claim 18, wherein the lightly doped regions are doped with an n-type impurity and a p-type impurity.

25. The lateral semiconductor device according to Claim 19, wherein the width of the curved section is larger than the width of the straight section.

26. The lateral semiconductor device according to Claim 18, wherein the width of the lightly doped region is larger than the width of the alternating conductivity type layer.

27. The lateral semiconductor device according to Claim 18, further comprising one or more closed loops, each including one or more alternating conductivity type layers and lightly doped regions.

28. The lateral semiconductor device according to Claim 18, wherein the width of the first semiconductor region or the second semiconductor region is from 1/4 to 4 times as

large as the depth of the first semiconductor region or the second semiconductor region.

29. The lateral semiconductor device according to Claim 18, wherein the width of the alternating conductivity type layer is from 12.5 to 100 times as large as the width of the first semiconductor region or the second semiconductor region.

30. The lateral semiconductor device according to Claim 18, wherein the width of the alternating conductivity type layer is from 12.5 to 100 times as large as the depth of the first semiconductor regions or the second semiconductor regions.

31. The lateral semiconductor device according to Claim 1, wherein the lateral semiconductor device comprises a semiconductor device selected from the group consisting of a MOSFET, a bipolar transistor, an IGBT and a diode; the main electrode, the potential thereof is high, is inside the closed loop; and the other main electrode, the potential thereof is low, is outside the closed loop.

32. The lateral semiconductor device according to Claim 18, wherein the lateral semiconductor device comprises a semiconductor device selected from the group consisting of a MOSFET, a bipolar transistor, an IGBT and a diode; the main electrode, the potential thereof is high, is inside the closed loop; and the other main electrode, the potential thereof is low, is outside the closed loop.

33. The lateral semiconductor device according to Claim 1, further comprising a circuit for controlling the semiconductor device, for protecting the semiconductor device and for detecting the states of the semiconductor device, the circuit being outside the closed loop.

34. The lateral semiconductor device according to Claim 18, further comprising a circuit for controlling the semiconductor device, for protecting the semiconductor device and for detecting the states of the semiconductor device, the circuit being outside the closed loop.